1   1.   A memory array circuit comprising:

2   memory cells;

3   first read bit lines coupled to a first subset of the memory cells; and

4   first NAND gates coupled to the first read bit lines, wherein each of the first

5   NAND gates has two inputs that are coupled to two of the first read bit lines.

1   2.   The memory array according to claim 1 further comprising:

2   first transistors, each of the first transistors having an input coupled to an

3   output of one of the first NAND gates; and

4   a first global bit line coupled to each of the first transistors.

1   3.   The memory array according to claim 2 further comprising:

2   a second pull up transistor coupled to the first global bit line; and

3   third pull up transistors, wherein each of the third pull up transistors are

4   coupled to one of the first read bit lines, and the first transistors are pull down transistors.

1   4.   The memory array according to claim 2 further comprising:

2   second read bit lines coupled to a second subset of the memory cells; and

3   second NAND gates coupled to the second read bit lines, wherein each of the

4   second NAND gates has two inputs that are coupled to two of the second read bit lines.

1   5.   The memory array according to claim 4 further comprising:

2   second transistors, each of the second transistors having an input coupled to an

3   output of one of the second NAND gates; and

4   a second global bit line coupled to each of the second transistors.

1   6.   The memory array according to claim 5 further comprising:

2   a third NAND gate having a first input coupled to the first global bit line and a

3   second input coupled to the second global bit line.

1   7.   The memory array according to claim 5 further comprising:

2   a repeater circuit coupled between the first global bit line and the second

3   global bit line.

1   8.   The memory array according to claim 7 wherein:

2   the repeater circuit includes an inverter coupled to a third transistor.

1   9.   A memory array circuit comprising:

2   memory cells;

3   first local read bit lines coupled to a first subset of the memory cells;

4   first logic gates, each coupled to receive signals on two of the first local read

5   bit lines;

6   a first global bit line; and

7   first transistors coupled between the first global bit line and the first logic

8   gates.

1   10.   The memory array circuit according to claim 9 further comprising:

2   second local read bit lines coupled to a second subset of the memory cells;

3   second logic gates, each coupled to receive signals on two of the second local

4   bit lines;

5   a second global bit line; and

6   second transistors coupled between the second global bit line and the second

7   logic gates.

1   11.   The memory array according to claim 10 further comprising:

2   an inverter circuit coupled to the first global bit line; and

3   a third transistor coupled to the inverter circuit and the second global bit line.

1   12.   The memory array according to claim 10 wherein:

2   the first logic gates and the second logic gates are NAND gates.

1   13.   The memory array according to claim 10 further comprising:

2   a NAND gate having a first input coupled to the first global bit line and a

3   second input coupled to the second global bit line.

1   14.   The memory array circuit according to claim 9 further comprising:

2   a first pre-charge transistor coupled to the first global bit line; and

3   a plurality of second pre-charge transistors that are each coupled to one of the

4   first local read bit lines.

1   15.   A method for reading bits from memory cells in a memory array, the

2 method comprising:

3   accessing a first bit from a first memory cell on a first local read bit line;

4   transmitting a signal indicative of the first bit from the first local read bit line

5 to a first global bit line through a first logic gate;

6   accessing a second bit from a second memory cell on a second local read bit

7 line; and

8   transmitting a signal indicative of the second bit from the second local read bit

9 line to the first global bit line through the first logic gate.

1   16.   The method according to claim 15 wherein:

2   the first logic gate is a NAND gate.

1   17.   The method according to claim 15 wherein transmitting the signals

2 indicative of the first and the second bits further comprises:

3   transmitting the signals indicative of the first and the second bits from the first

4 logic gate to a transistor that is coupled to the first global bit line.

1   18.   The method according to claim 15 further comprising:

2   accessing a third bit from a third memory cell on a third local read bit line;

3   transmitting a signal indicative of the third bit from the third local read bit line

4 to the first global bit line through a second logic gate;

5   accessing a fourth bit from a fourth memory cell on a fourth local read bit line;

6 and

7   transmitting a signal indicative of the fourth bit from the fourth local read bit

8 line to the first global bit line through the second logic gate.

1   19.   The method according to claim 15 further comprising:

2   accessing a third bit from a third memory cell on a third local read bit line;

3   transmitting a signal indicative of the third bit from the third local read bit line

4 to a second global bit line through a second logic gate;

5   accessing a fourth bit from a fourth memory cell on a fourth local read bit line;

6 and

7   transmitting a signal indicative of the fourth bit from the fourth local read bit

8 line to the second global bit line through the second logic gate.

1   20.   The method according to claim 19 further comprising:

2   transmitting the signal indicative of the first bit from the first global bit line to

3 the second global bit line through a repeater circuit.

1   21.   The method according to claim 20 wherein the repeater circuit

2 comprises an inverter coupled to the gate of a field effect transistor, and the field effect

3 transistor pulls down the voltage on the second global bit line.

1   22.   The method according to claim 19 wherein:

2   the first and the second logic gates are NAND gates.

1   23.   The method according to claim 19 further comprising:

2   transmitting a signal indicative of the first bit or the second bit from the first

3 global bit line to a third level bit line through a NAND gate; and

4   transmitting a signal indicative of the third bit or the fourth bit from the second

5 global bit line to the third level bit line through the NAND gate.